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(19) **United States**(12) **Patent Application Publication****Chan et al.**(10) **Pub. No.: US 2014/0299882 A1**(43) **Pub. Date: Oct. 9, 2014**(54) **INTEGRATED FIN AND STRAP STRUCTURE
FOR AN ACCESS TRANSISTOR OF A
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Corporation**, Armonk, NY (US)(21) Appl. No.: **13/857,282**(22) Filed: **Apr. 5, 2013****Publication Classification**(51) **Int. Cl.**
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(2013.01)USPC **257/66; 438/155**(57) **ABSTRACT**

At least one dielectric pad layer is formed on a semiconductor-on-insulator (SOI) substrate. A deep trench is formed in the SOI substrate, and a combination of an outer electrode, a node dielectric, and an inner electrode are formed such that the top surface of the inner electrode is recessed below the top surface of a buried insulator layer of the SOI substrate. Selective epitaxy is performed to fill a cavity overlying the inner electrode with an epitaxial semiconductor material portion. A top semiconductor material layer and the epitaxial semiconductor material portion are patterned to form a fin structure including a portion of the top semiconductor material layer and a portion of the epitaxial semiconductor material portion. The epitaxial semiconductor material portion functions as a conductive strap structure between the inner electrode and a semiconductor device to be formed on the fin structure.

